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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/437,135	11/10/1999	SHUNPEI YAMAZAKI	0756-2064	7576

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EXAMINER	
KIELIN, ERIK J	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)
	09/437,135	YAMAZAKI ET AL.
	Examiner	Art Unit
	Erik Kielin	2813

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 29-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 29-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *18* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 22 January 2002 has been entered.

Information Disclosure Statement

2. The information disclosure statement filed 20 December 2001 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered. More specifically, the application 49-78483 has not been considered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **1**-4, **6**-9, **30**-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,274,279 (**Misawa** et al.) in view of Applicant's admitted prior art (**APA**) and the article

Ang et al. "Electrical characterization of low-pressure chemical-vapor-deposited silicon dioxide metal-oxide-silicon structures" Journal of Applied Physics 73(5), 1 March 1993, pp. 2397-2401.

Regarding independent claims 1, 6, and 30, **Misawa** discloses a method of forming semiconductor devices, which are CMOS TFTs, comprising the steps of,

forming first, second, and third, patterned, crystallized col. 9, lines 19-26), silicon semiconductor islands **111**, **112**, **113** over a transparent substrate **110** (Figs. 4A; col. 7, lines 60-66);

forming gate insulating films **114**, **115**, **116** formed from silicon oxides (as further limited by instant claims 6 and 30; col. 6, lines 39-46) on each of the semiconductor islands using chemical vapor deposition (Fig. 4A; sentence bridging cols. 7-8);

forming gate electrodes **117**, **118**, **119** on each of the gate insulating films (Fig. 4A; sentence bridging cols. 7-8);

introducing phosphorous into said first and second semiconductor islands and introducing boron into said second semiconductor island, wherein a dose amount of said boron is larger than that of said phosphorous (col. 8, lines 3-56 -- **especially lines 50-56)**.

Misawa is silent to the method by which the semiconductor islands are formed, but as noted above indicates that they are polycrystalline at col. 9, lines 19-26.

The **APA** discloses that it is known in the art to make a TFT by forming a semiconductor film comprising amorphous silicon over a substrate; crystallizing said semiconductor film by irradiating a laser light. (Applicant's specification, pages 2-4). It would have been obvious for one of ordinary skill in the art, at the time of the invention to apply the silicon islands **111**, **112**, **113** of **Misawa** by depositing amorphous silicon and laser crystallizing as taught by **APA**,

because **Misawa** is silent to the method by which such polycrystalline patterned silicon islands are formed, such that one of ordinary skill would be motivated to use known methods for forming such as that taught by **APA** to be known specifically for TFTs such as **Misawa** is making.

Then the only difference is that **Misawa** does not teach that the gate insulating layers of silicon oxides **114**, **115**, **116**, disclosed therein as deposited by CVD, are irradiated by an intense light, in an atmosphere comprising oxygen gas.

Ang teaches the benefits of depositing an insulating layer for a gate oxide using low pressure CVD (instant claims 3, 8, and 32) and then thermally annealing in oxygen using a Heatpulse 210T rapid thermal processor which emits high intensity IR light (instant claims 2, 7, and 31) (see attached document, page 1, from UC-Berkeley obtained by the Internet for verification) in order to reduce the interfacial layer density (called both "fixed charge density" and "interface state density" therein) to well below 10^{11} cm^{-2} (instant claims 4, 9, and 33). (See Abstract and section entitled "Experiment.") It would have been obvious to one of ordinary skill in the art at the time the invention was made to irradiate the gate dielectric of **Misawa**, in accordance with the teaching in **Ang** for the numerous benefits taught by **Ang**. It would further be obvious to use low pressure CVD as the CVD of **Misawa,** because **Misawa** is silent to which CVD method is used to deposit the gate insulating silicon oxide, such that one of ordinary skill would be motivated to use the entire teaching of **Ang** since **Ang** shows that the low pressure CVD gate oxides should be laser annealed.

5. Claims **11**-13, 29, and **34**-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,274,279 (**Misawa** et al.) in view of the **APA** and **Ang** and further in view of **Wolf**, et al. Silicon Processing for the VLSI Era, Vol. 1-Process Technology, Lattice Press: Sunset Beach CA, 1986, pp. 183-184.

The prior art of **Misawa** in view of the **APA**, as explained above, discloses each of the claimed features except for using TEOS as the CVD precursor gas to form the gate insulating layer.

Wolf teaches that TEOS is a known CVD precursor gas for depositing silicon oxide insulating layers which provides excellent step coverage ("conformality"), as would be required over the semiconductor islands. (See especially p. 184, last full paragraph.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use TEOS as the precursor gas of **Misawa**, because **Misawa** is silent as to which precursor gas is used, such that one of ordinary skill would be motivated to find known CVD precursor gases, especially ones providing excellent step coverage, since the **Misawa** semiconductor islands create topography (e.g. steps) thereby requiring excellent step coverage ("conformality"), as taught in **Wolf** as appropriate for TEOS.

6. Claims **1**-4, **6**-9, **11**-13, 29, **30**-33, and **34**-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Misawa** in view of Applicant's **APA** and **Roy** (US 5,153,701) and **Wolf** (Silicon Processing for the VLSI Era, Vol. 1, Lattice Press: Sunset Beach, CA, 1986, pp. 57-58) or alternatively in view of **APA** and **Roy** and **JP 58-098933**.

Misawa in view of the **APA** is applied as above.

The prior art of **Misawa** in view of the **APA**, as explained above, discloses each of the claimed features except for using TEOS as the CVD precursor gas to form the gate insulating layer and then the irradiating the gate insulating silicon oxide using a high intensity light in an oxygen atmosphere.

Roy teaches the benefits of using LPCVD or PECVD and TEOS to form an insulating film comprising SiO_2 on a semiconductor film for use as a gate electrode and then annealing in oxygen for the express purpose of reducing interfacial layer density (called "charge traps" or "interface trap density" therein) to a level inherently below 10^{11} cm^{-2}. (See column 2, lines 16-21; column 3, lines 23-44; column 7, line 41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate insulating silicon oxide of **Misawa** to use TEOS as the CVD precursor gas and then to anneal in an oxygen atmosphere, as taught by **Roy** for the reasons indicated in **Roy**, or specifically annealing in oxygen to reduce interfacial layer density. The use of TEOS is also obvious because **Misawa** is silent to the CVD precursor gas for the **Misawa** CVD method, such that one of ordinary skill would be motivate to follow the entire teaching of **Roy** and use TEOS as the CVD precursor gas.

Then the only difference is that high intensity light as the annealing heat source is not taught in **Misawa** in view of **Roy**.

Wolf teaches the benefits of rapid thermal annealing using high intensity IR. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the high intensity IR annealing method of **Wolf** for the **Roy** annealing source of heat for the reasons in **Wolf**, especially to reduce thermal budget which is especially important in TFT processing, as indicated in the **APA**.

Alternatively, **JP 58-098933** teaches the benefits of using CVD to deposit an insulating film comprising SiO_2 on a silicon substrate, followed by UV, IR or laser annealing to expressly reduce the interfacial layer density (called "boundary level density" therein). (See Abstract and Derwent Abstract.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to use IR light as the annealing method in **Roy** for the reasons in **JP 58-098933,** which include specifically to reduce the interfacial state density at the Si/SiO_2 interface of CVD deposited SiO_2 in concert with the teaching in **Roy**.

7. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Misawa** in view of the **APA** and **Ang**, as applied to claims 1-4 and 6-9 above, and further in view of **JP 60-187030**.

Misawa in view of the **APA** and **Ang** does not indicate the kind of laser to be used for crystallizing the silicon film.

JP 60187030 discloses the benefits of Applicant's claimed laser for such crystallizing (Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to crystallize the silicon using the lasers in **JP 60187030** for the reasons indicated therein.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Misawa** in view of the **APA** and **Ang** and **Wolf**, as applied to claims 11-13 above, and further in view of **JP 60-187030**.

Misawa in view of the **APA** and **Ang** does not indicate the kind of laser to be used for crystallizing the silicon film.

JP 60187030 is applied as above.

9. Claims 5, 10, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Misawa** in view of the **APA** and **Roy** and **Wolf** or alternatively over **Misawa** in view of the **APA** and **Roy** and **JP 58-098933**, either of the above as applied to claims 1-4, 6-9, and 11-13 above, and further in view of **JP 60-187030**.

Misawa in view of the **APA** and **Roy and Wolf** or, alternatively, in view of **APA** and **Roy** and **JP 58-098933** does not indicate the kind of laser to be used for crystallizing the silicon film.

JP 60187030 is applied as above.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,116,771 (**Karulkar**) and US 4,996,575 (**Ipri** et al.) each disclose CMOS TFTs formed from crystalline semiconductor islands with the doping as presently claimed.

Any inquiry concerning this communication from examiner should be directed to Erik Kielin whose telephone number is (703) 306-5980 and e-mail address is erik.kielin@uspto.gov. The examiner can normally be reached by telephone on Monday through Thursday 9:00 AM until 7:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached at (703) 306-2794 or by e-mail at olik.chaudhuri@uspto.gov. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

EK

EK

August 7, 2002

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